pair of wirings that needs to be electrically connected to each other, and a corresponding area as a projection of the setting area is provided on the other wiring. With this arrangement, a through-hole is set in a shape that pierces through the insulation layer, and the setting area and the corresponding areas are connected to each other.

Replace the paragraph beginning at page 3, line 21 with:

However, along with the request for making devices smaller in recent years, there has been progress in reduction in the size of a circuit element and a reduction in the width of wiring. As shown in Fig. 11, a through-hole is set to have a smaller width than that of wiring. Therefore, a cross-sectional area of one through-hole per circuit surface also becomes smaller, corresponding to the reduction in the wiring width. Further, according to the conventional automatic wiring, only one through-hole for electric conduction is provided for a pair of wirings that are disposed in different layers.

Replace the paragraph beginning at page 4, line 6 with:

The electric resistance of a through-hole is inversely proportional to cross-sectional area of the through-hole. Therefore, as the reduction in size of a semiconductor integrated circuit has progressed, the resistance of the through-hole has increased, and a current flow has become more difficult.

Replace the paragraph beginning at page 4, line 24 with:

Further, in general, it has been known that electromigration resistance is lowered in inverse proportion to the square of current density. The current density of a through-hole having a smaller cross-section increases when the same level of current flows. This brings about a problem in that the electromigration resistance is lowered.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number